Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (original): A data transmission circuit comprising:

a control signal generation circuit, which receives a strobe signal and a clock signal, which generates a write control signal that is activated in response to the strobe signal, and which generates a read control signal that is activated in response to a first rising or falling edge of the clock signal after the write control signal is activated;

a write state machine which is activated in response to the write control signal, which internally synchronizes with the strobe signal, and which sequentially outputs a plurality of input control signals;

a conversion circuit which latches serial input data at a timing of the input control signals to converts the input serial data into parallel latched data;

a read state machine which is activated in response to the read control signal, which internally synchronizes with the clock signal, and which sequentially outputs a plurality of output control signals; and

a selection circuit which selects the parallel latched data in response to the output control signals, and which outputs the selected data as serial output data which has the same data order as the serial input data.

Claim 2 (original): The data transmission circuit of claim 1, wherein the conversion circuit includes a plurality of flip-flops which respectively receive the input control signals, wherein each of the plurality of flip-flops latches the serial data in response to a respective input control signal.

Claim 3 (currently amended): The data transmission circuit of claim 1, wherein ~~a~~ the read state machine initiates internal synchronization with the clock signal in response to the first rising or falling edge of the clock signal after the read control signal is activated.

Claim 4 (original): The data transmission circuit of claim 1, wherein a latency of the output serial data relative to the input serial data is one data bit period.

Claim 5 (currently amended): The data transmission circuit of claim ~~1~~ 4, wherein the one data bit period is one-half a period of the clock signal.

Claim 6 (original): A control signal generation circuit comprising:
a first input terminal which receives a strobe signal;
a second input terminal which receives a clock signal;
a control terminal which receives an enable signal;
a first output terminal which outputs a write control signal;
a second output terminal which outputs a read control signal; and
a third output terminal which outputs a selection signal,
wherein the control signal generation circuit is configured to receive the strobe signal and the clock signal in response to the enable signal being activated, to generate the write control signal that is activated in response to the strobe signal, to generate the read control signal that is activated in response to a first rising or falling edge of the clock signal after the write control signal is activated, to compare a phase of the strobe signal with a phase of the clock signal, and to output the selection signal according to a result of the phase comparison.

Claim 7 (currently amended): The control signal generation circuit of claim [[4]] 6, further comprising:

a first latch which latches the enable signal in synchronization with the strobe signal;

a second latch which latches an output signal of the first latch in synchronization with a complementary signal of the strobe signal;

a third latch which outputs an output signal of the second latch as the write control signal in synchronization with the strobe signal;

a fourth latch which latches the enable signal in synchronization with the clock signal;

a fifth latch which latches an output signal of the fourth latch in synchronization with a complementary signal of the clock signal;

a sixth latch which latches an output signal of the fifth latch in synchronization with the clock signal;

a seventh latch which latches an output signal of the sixth latch in synchronization with the complementary signal of the clock signal;

an eighth latch which latches an output signal of the seventh latch in synchronization with the strobe signal;

a first set-reset (S-R) latch which receives the output signals of the first and fourth latches;

a second S-R latch which receives the output signals of the second and fourth latches;

a third S-R latch which receives the output signals of the first and fifth latches;

a first exclusive OR (XOR) gate which receives output signals of the first and third S-R latches;

a second XOR gate which receives output signals of the first S-R latch and the first XOR gate and outputs an XOR operation result of the output signals of the first S-R latch and the first XOR gate as the selection signal; and

a multiplexer which outputs one of the output signals of the fifth through eight latches as the read control signal in response to combinations of the output signals of the first and second XOR gates.

Claim 8 (currently amended): A data transmission circuit comprising:

control signal generation circuit comprising (a) a first input terminal which receives a strobe signal, (b) a second input terminal which receives a clock signal, (c) a control terminal which receives an enable signal, (d) a first output terminal which outputs a write control signal, (e) a second output terminal which outputs a read control signal, (f) and a third output terminal which outputs a selection signal, and wherein the control signal generation circuit is configured to receive the strobe signal and the clock signal in response to the enable signal being activated, to generate the write control signal that is activated in response to the strobe signal, to generate the read control signal that is activated in response to a first rising or falling edge of the clock signal after the write control signal is activated, to compare a phase of the strobe signal with a phase of the clock signal, and to output the selection signal according to a result of the phase comparison[[.]];

a write state machine which is activated in response to the write control signal, which internally synchronizes with the strobe signal, and which sequentially outputs a plurality of input control signals;

a conversion circuit which latches serial input data at a timing of the input control signals to converts the input serial data into parallel latched data;

a read state machine which is activated in response to the read control signal, which internally synchronizes with a rising or falling edge of the clock signal based on the selection signal, and which sequentially outputs a plurality of output control signals; and

a selection circuit which selects the parallel latched data in response to the output control signals, and which outputs the selected data as serial output data which has the same data order as the serial input data.

Claim 9 (original): The data transmission circuit of claim 8, wherein the conversion circuit includes a plurality of flip-flops which respectively receive the input control signals, wherein each of the plurality of flip-flops latches the serial data in response to a respective input control signal.

Claim 10 (original): The data transmission circuit of claim 8, wherein a latency of the output serial data relative to the input serial data is one data bit period.

Claim 11 (currently amended): The data transmission circuit of claim [[8]] 10, wherein the one data bit period is one-half a period of the clock signal.

Claim 12 (original): A data transmission circuit comprising:

a control signal generation circuit which receives a strobe signal and a clock signal in response to an enable signal being activated, which generates a write control signal that is activated in response to the strobe signal, which generates a read control signal that is activated in response to a first rising or falling edge of the clock signal after the write control signal is activated, which compares a phase of the strobe signal with a phase of the clock signal, and which outputs a selection signal according to a result of the phase comparison;

a write state machine which is activated in response to the write control signal, which internally synchronizes with the strobe signal, and which sequentially outputs a plurality of input control signals;

a conversion circuit which latches serial input data at a timing of the input control signals to converts the input serial data into parallel latched data;

a read state machine which is activated in response to the read control signal, which internally synchronizes with a rising or falling edge of the clock signal based on the selection signal, and which sequentially outputs a plurality of output control signals; and

a selection circuit which selects the parallel latched data in response to the output control signals, and which outputs the selected data as serial output data which has the same data order as the serial input data.

Claim 13 (original): The data transmission circuit of claim 12, wherein a latency of the output serial data relative to the input serial data is one data bit period.

Claim 14 (original): The data transmission circuit of claim 13, wherein the one data bit period is one-half a period of the clock signal.

Claim 15 (original): A method of transmitting data, the method comprising:

receiving a strobe signal and a clock signal in response to an enable signal, generating a write control signal that is activated in response the strobe signal, and generating a read control signal that is activated in response to a first rising or falling edge of the clock signal which occurs after the write control signal is activated;

internally synchronizing, in response to the write control signal, with the strobe signal and sequentially outputting input control signals;

latching serial input data at a timing of the input control signals to converts the input serial data into parallel latched data;

internally synchronizing, in response to the read control signals, with the clock signal and sequentially outputting output control signals; and

selecting the parallel latched data in response to the output control signals, and outputting the selected data as serial output data which has the same data order as the serial input data.

Claim 16 (original): The method of claim 15, wherein said sequentially outputting the output control signals is characterized by initiating internal

synchronization with the clock signal in response to a first rising or falling edge of the clock signal after the read control signal is activated.

Claim 17 (original): The method of claim 15, wherein a latency of the output serial data relative to the input serial data is one data bit period.

Claim 18 (original): A method of transmitting data, the method comprising:

receiving a strobe signal and a clock signal in response to an enable signal, generating a write control signal that is activated in response the strobe signal, and generating a read control signal that is activated in response to a first rising or falling edge of the clock signal which occurs after the write control signal is activated, comparing a phase of the strobe signal with a phase of the clock signal, and outputting a selection signal according to result of the phase comparison;

internally synchronizing, in response to the write control signal, with the strobe signal and sequentially outputting input control signals;

latching serial input data at a timing of the input control signals to converts the input serial data into parallel latched data;

internally synchronizing, in response to the read control signals, with a rising or falling edge of the clock signal based on the selection signal and sequentially outputting output control signals; and

selecting the parallel latched data in response to the output control signals, and outputting the selected data as serial output data which has the same data order as the serial input data.

Claim 19 (original): The method of claim 18, wherein a latency of the output serial data relative to the input serial data is one data bit period.